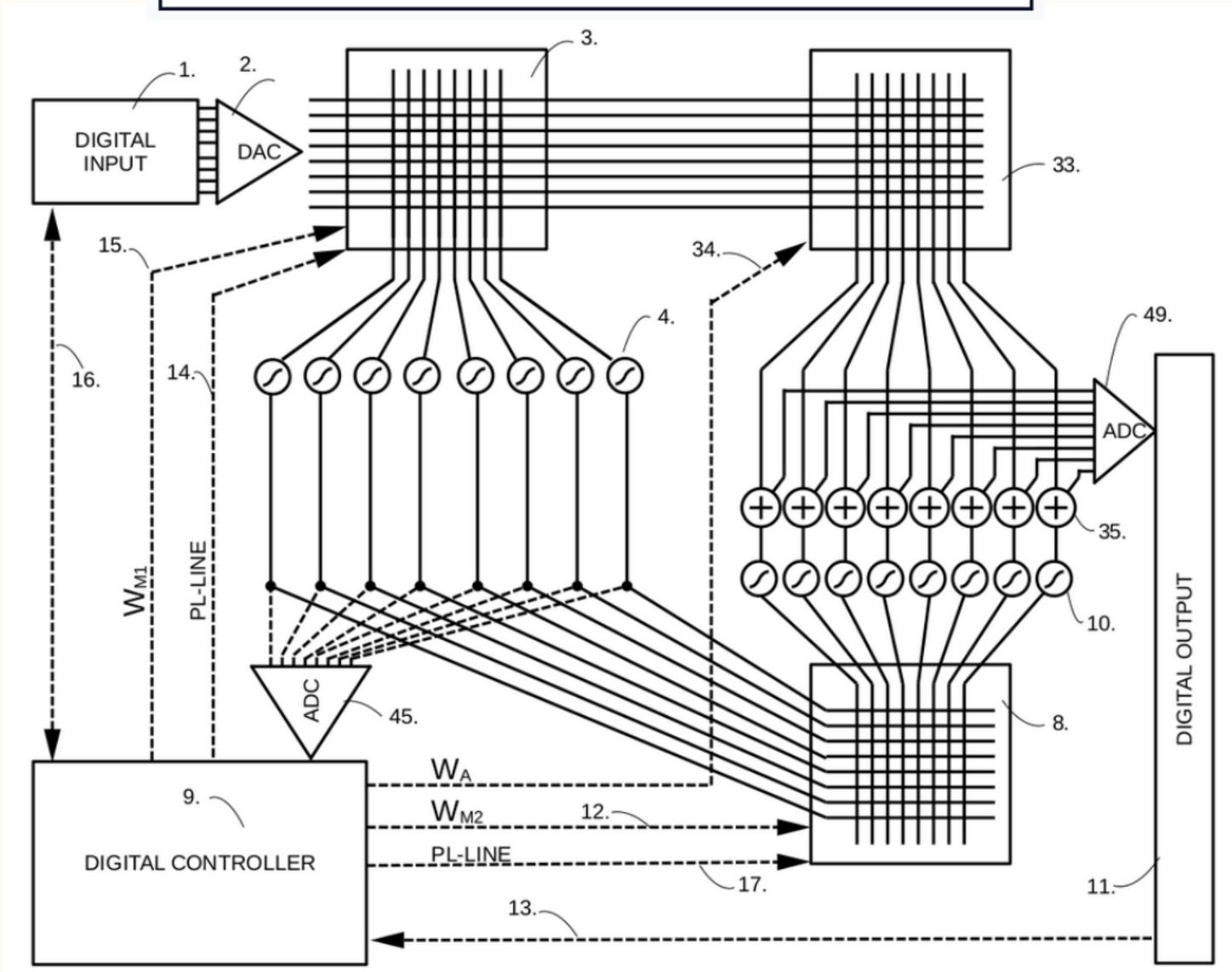
TITLE: INVERTED MAML FOR ANALOG IMC MESH

PATENT APP NO: SE 2630397-4

STATUS: PATENT PENDING

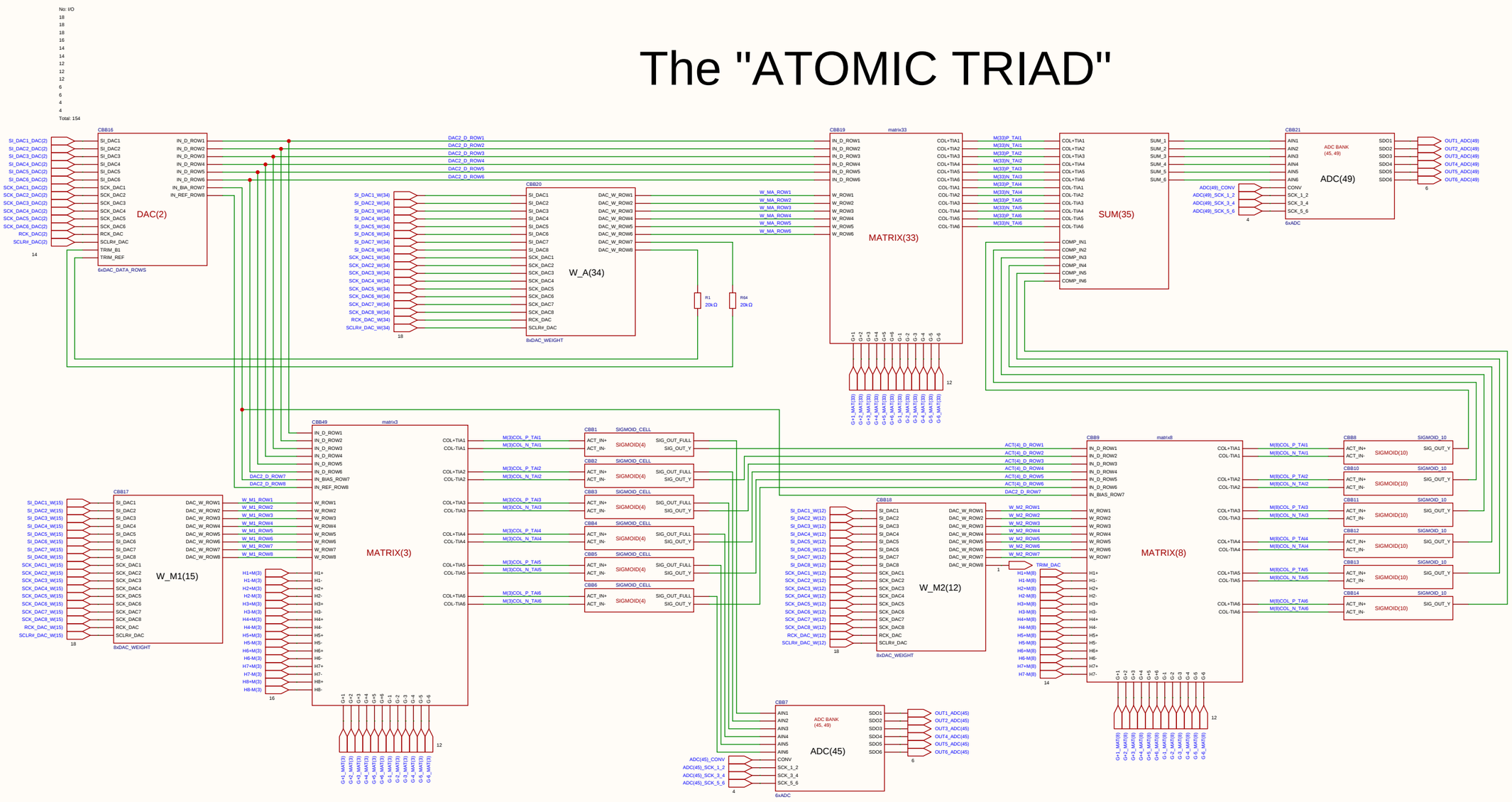
INVENTOR: OLLE WELIN

PRIORITY DATE: 2026-06-03



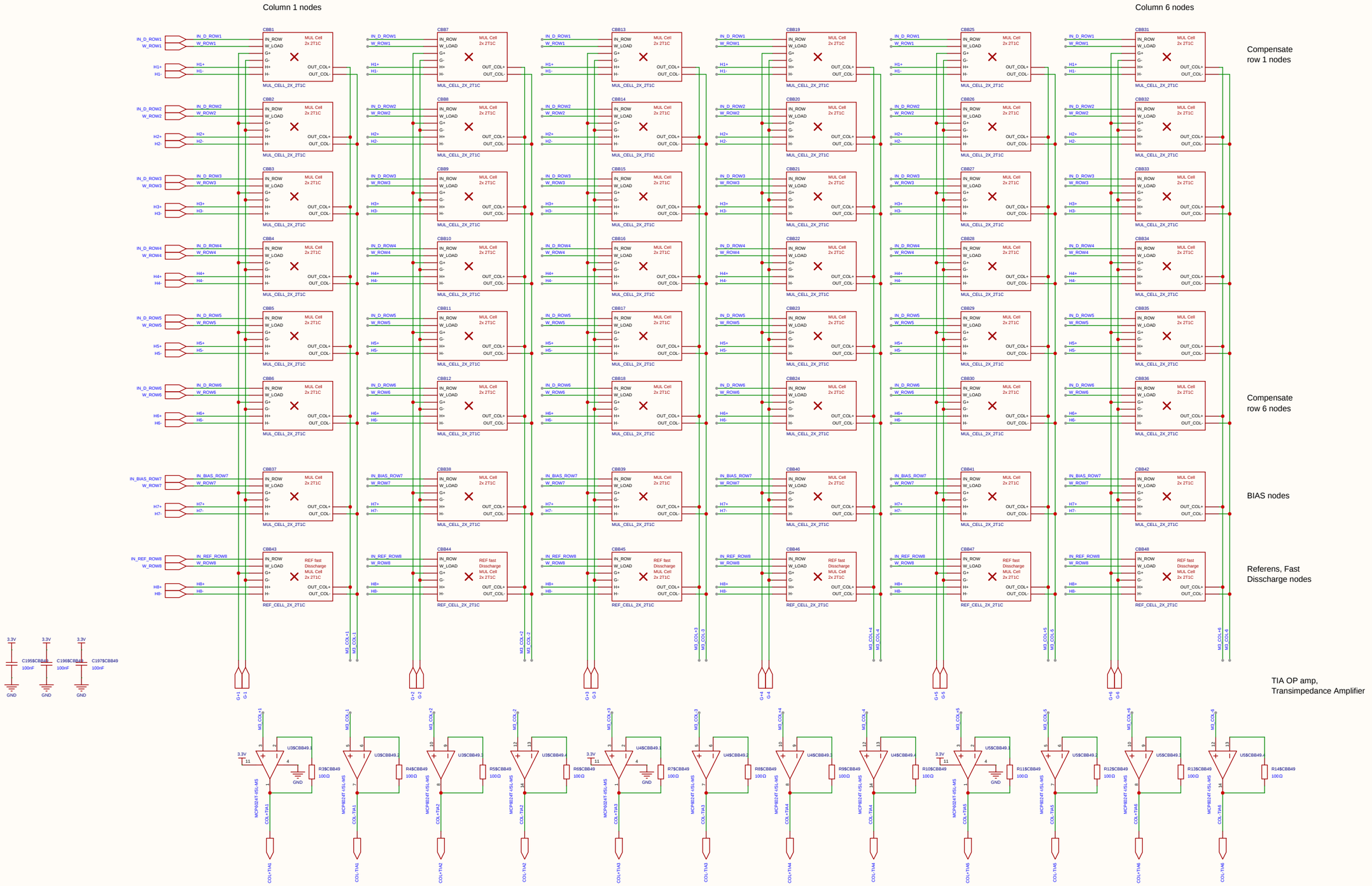
Schematic	Inverted_MAML	Create at	2026-06-19
		Update at	2026-06-19
Board	Analog_Matrix	Page	cover
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 3
EasyEDA		V1.0	A4	EasyEDA.com

The "ATOMIC TRIAD"



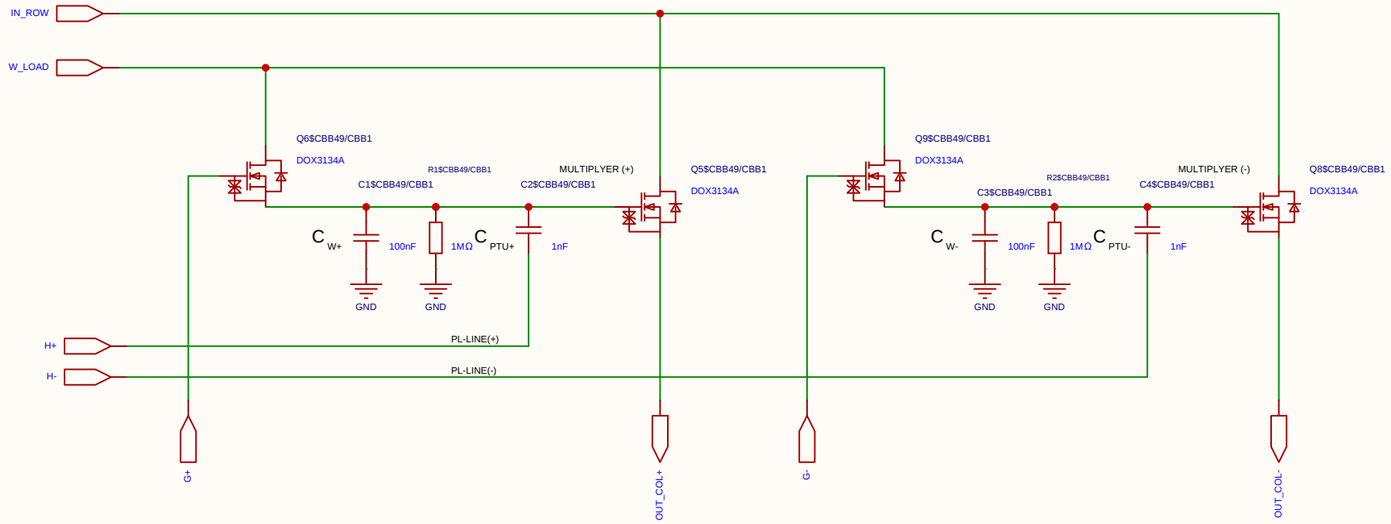
Schematic	Inverted_MAML	Create at	2026-06-25
		Update at	2026-06-27
Board	Analog_Matrix	Page	Atomic_Triad
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 2 Total 3
EasyEDA		V1.0	A4	EasyEDA.com

$$V_{ut_TIA} = 1.65\ \text{V} - (5\ \text{mA} \times 100\ \Omega) = 1.65\ \text{V} - 0.5\ \text{V} = \mathbf{1.15}\ \text{V}$$



Schematic	matrix3	Create at	2026-06-25
		Update at	2026-06-27
Board		Page	matx3
Drawn		Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

Analog Multiplication CELL Kernel
Differential 2x 2T1C



Category	Parameter	Value / Type	Technical Description & Function
Timing	Refresh cycle	**10 ms**	Total period time between cell weight updates.
	Refresh window	**≤ 100 µs**	Time allocated to charge the cell (95% reached in ~30 µs).
	Sampling time	**2 µs**	Throughput time for matrix multiplication per compute sample.
Voltages	Data swing (Row / V_{ds})	**250 mV**	Mapped from 1.65 V (0) to 1.90 V (255) for linear triode operation.
	Weight swing (Gate / V_{gs})	**1.0 V**	Swings from 2.1 V (Weight 0) to 3.1 V (Weight 255).
	Source potential (V_s)	**1.65 V**	Central reference point (Virtual Ground) for differential stage.
	Voltage drop (Droop)	**~9.5%**	Controlled voltage drop (~0.1 V) over a 10 ms period.
Components	Transistor	**DOX3134A**	N-channel trench MOSFET optimized for analog multiplication.
	Operational Amplifier	**MCP6024T**	Quad 10 MHz OP-amp used as a driving stage/ buffer.
	Weight capacitor (C)	**100 nF**	Local analog storage of the weight voltage in the 2T1C cell.

Category	Parameter	Value / Type	Technical Description & Function
	Discharge resistor (R)	**1 MΩ**	Sets the leakage rate in parallel across the capacitor.
	Series resistor (R_s)	**100 Ω**	Isolates the OP-amp from capacitive load; prevents oscillation.

1. Capacitors (Per Cell)

COMPONENT	VALUE	DESCRIPTION / FUNCTION
Weight Capacitor (C_W)	100 nF	Stores the analog weight voltage (V_{weight}). Swings from 2.1 V to 3.1 V (1.0 V total dynamic range).
Perturbation Capacitor (C_{PTU})	1 nF	Capacitive coupling capacitor. Forms a ~1/101 voltage divider against C_W to inject the Hadamard perturbation. Ensures non-destructive read operations.

4. Voltage Levels on the PL Row

STATE	PL VOLTAGE	PERTURBATION AT GATE	COMMENT
Idle State (Tri-state)	1.65 V	0 mV	Perfect center potential. Prevents noise pickup and ensures absolute charge neutrality.
Hadamard (+)	2.44 V	+15.6 mV	Exactly 1/64 of the 1.0V weight swing. Fully settled in under 2 µs.
Hadamard (-)	0.86 V	-15.6 mV	Mathematically symmetrical negative step for differential disturbance analysis.

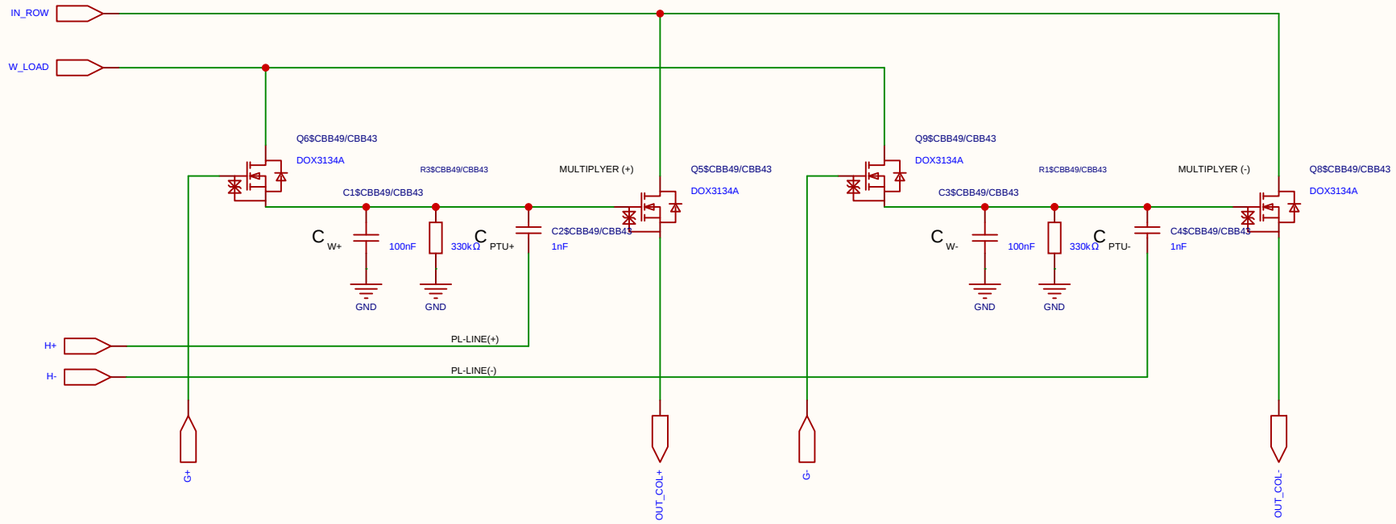
2. Resistor Network (Per PL Row)

This network connects the FPGA output pin to the PL_i row line (which drives 6 parallel C_{PTU} capacitors). It determines the perturbation amplitude and sets the RZ idle voltage.

COMPONENT	VALUE	DESCRIPTION / FUNCTION
Pull-up Resistor (R_1)	220 Ω	Connected between 3.3V and PL_i. Part of the idle state biasing (Return-to-Zero).
Pull-down Resistor (R_2)	220 Ω	Connected between GND (0V) and PL_i. Establishes exactly 1.65 V (V_s) during Tri-state.
Series Resistor (R_{series})	120 Ω	Connected between the FPGA pin and PL_i. Acts as dampening and attenuates the digital swing to achieve the targeted perturbation amplitude.

Schematic	MUL_CELL_2X_2T1C	Create at	2026-06-19
		Update at	2026-06-19
Board		Page	matrix_3_8_MUL_CELL
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

Analog REF DISSCHARGE
Multiplication CELL Kernel
Differential 2x 2T1C



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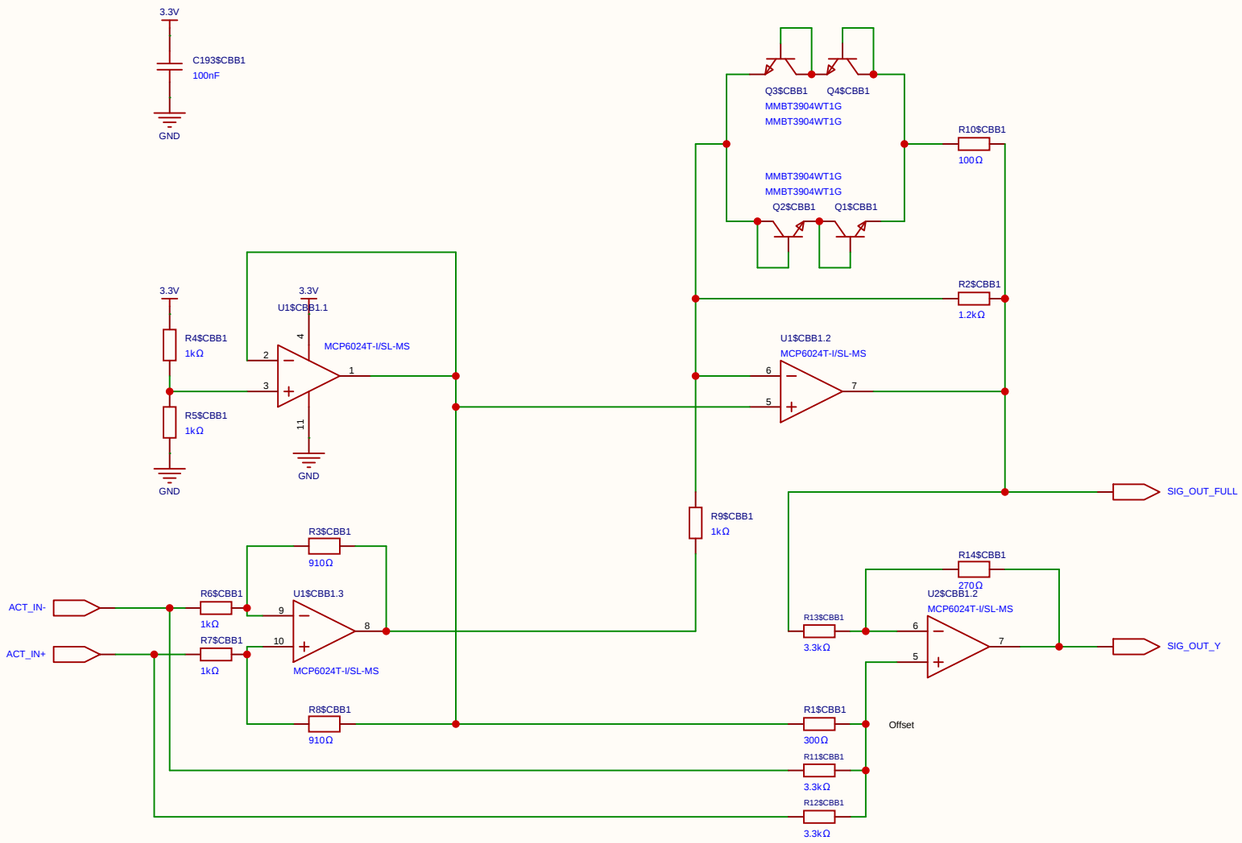
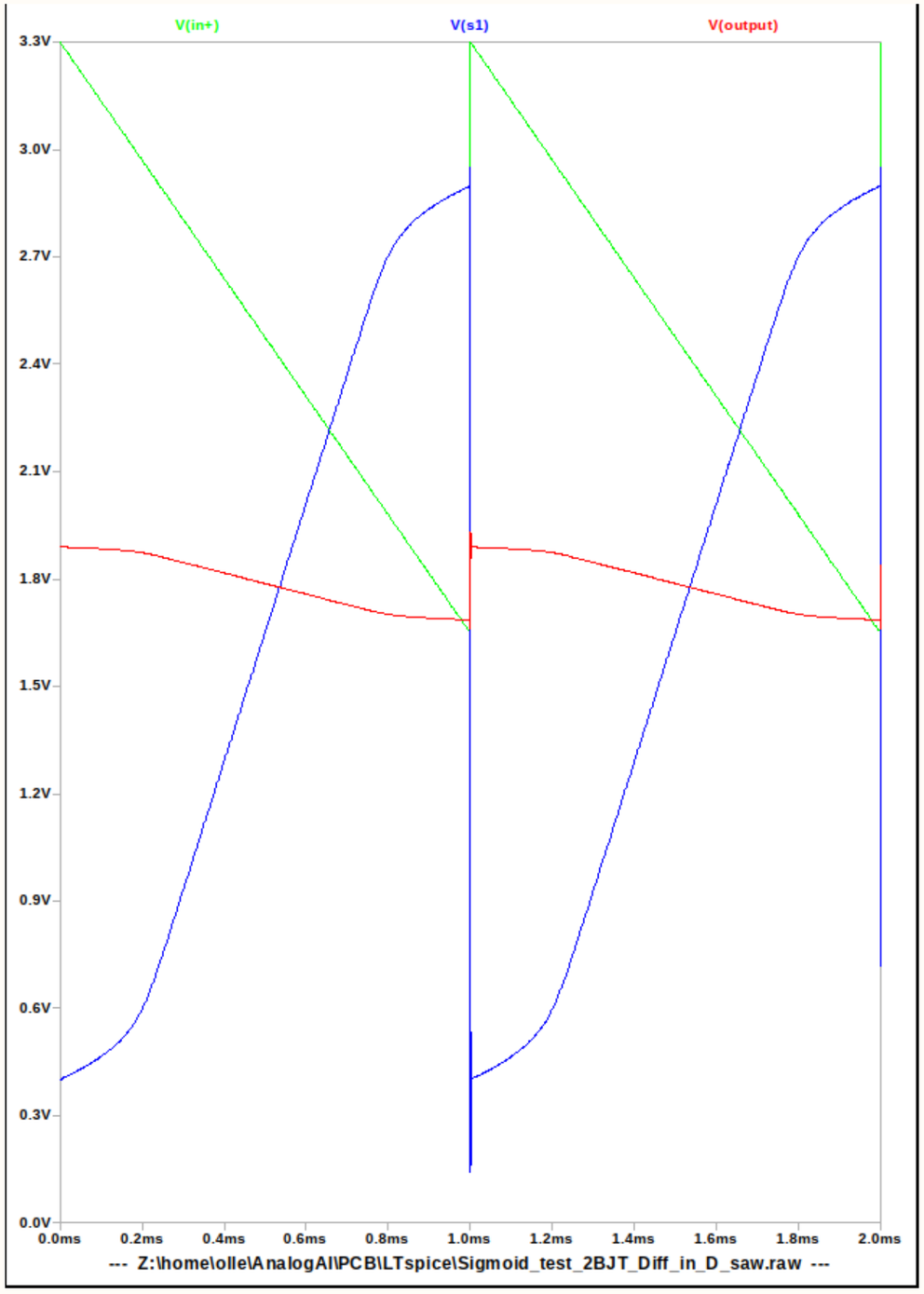
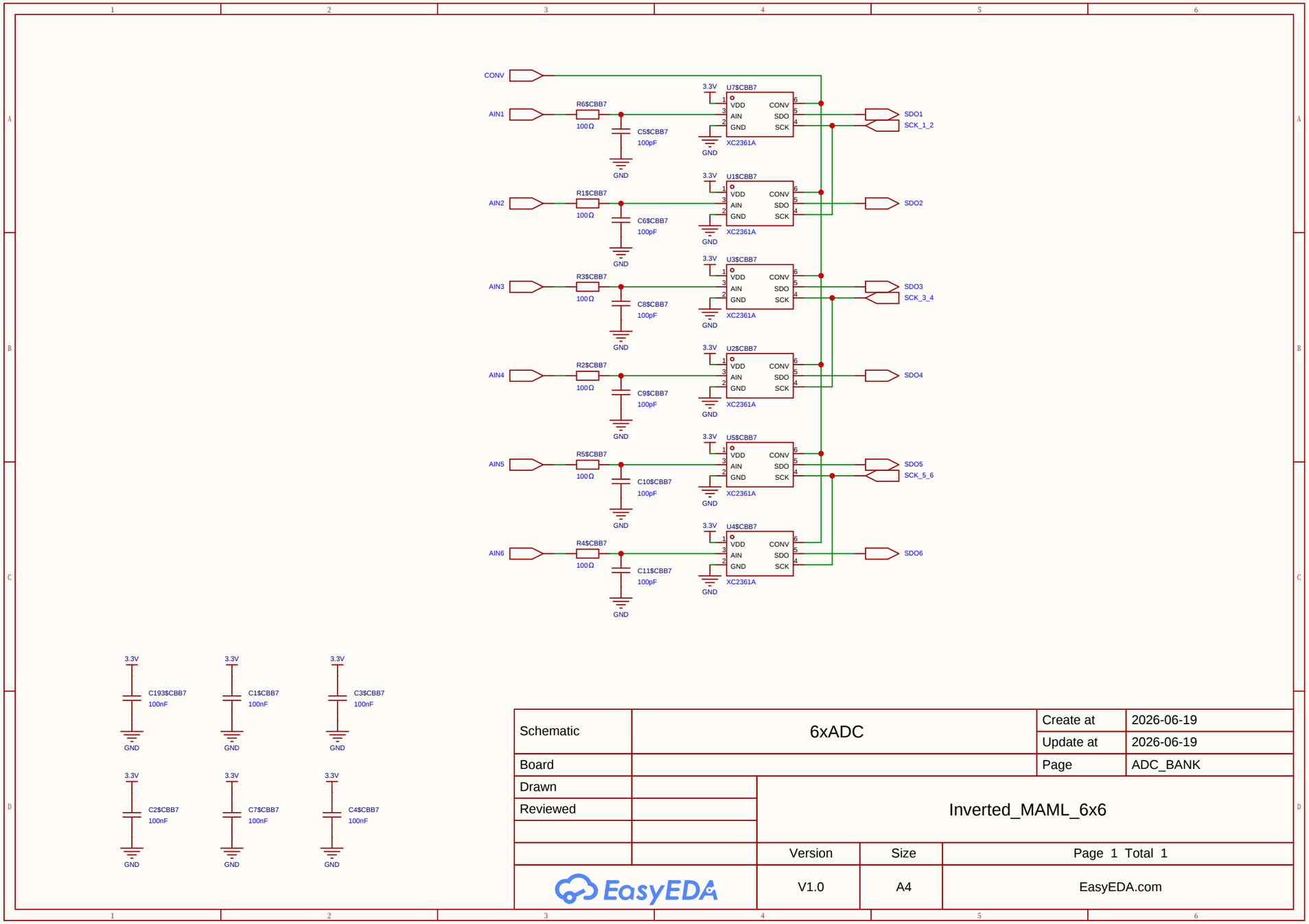
Schematic	REF_CELL_2X_2T1C	Create at	2026-06-19
		Update at	2026-06-30
Board		Page	matrix_3_REF_CELL
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

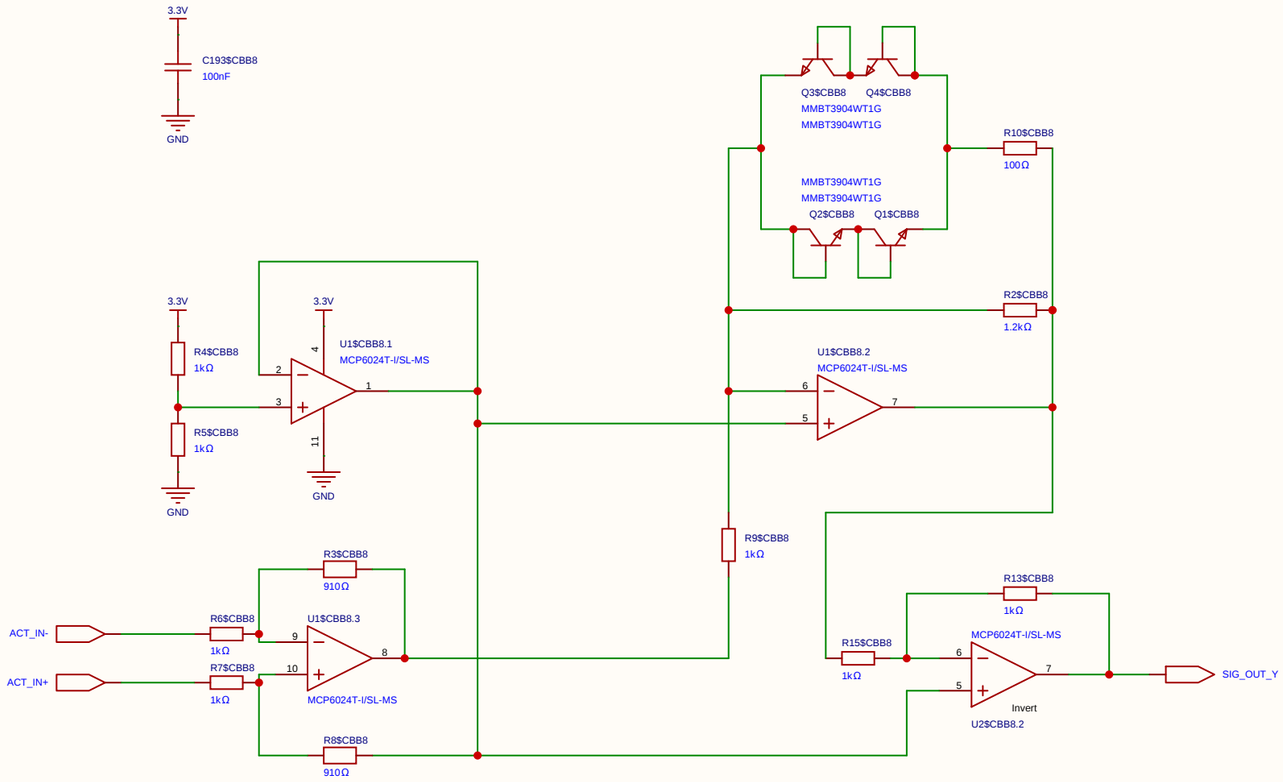




Schematic	SIGMOID_CELL	Create at	2026-06-19
		Update at	2026-06-19
Board		Page	SIMOID(4)
Drawn		Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

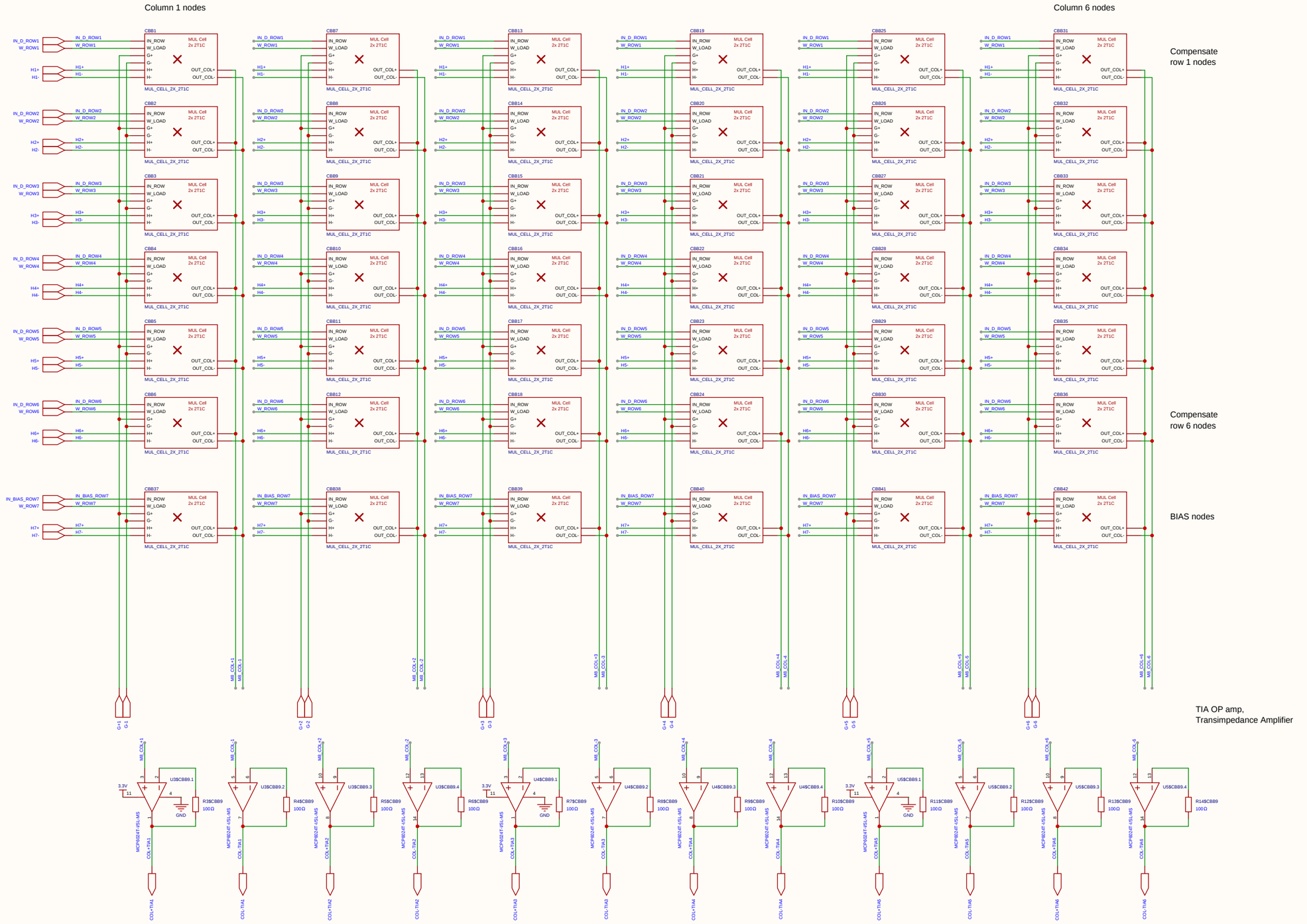


Schematic	6xADC	Create at	2026-06-19
		Update at	2026-06-19
Board		Page	ADC_BANK
Drawn	Inverted_MAML_6x6		
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com



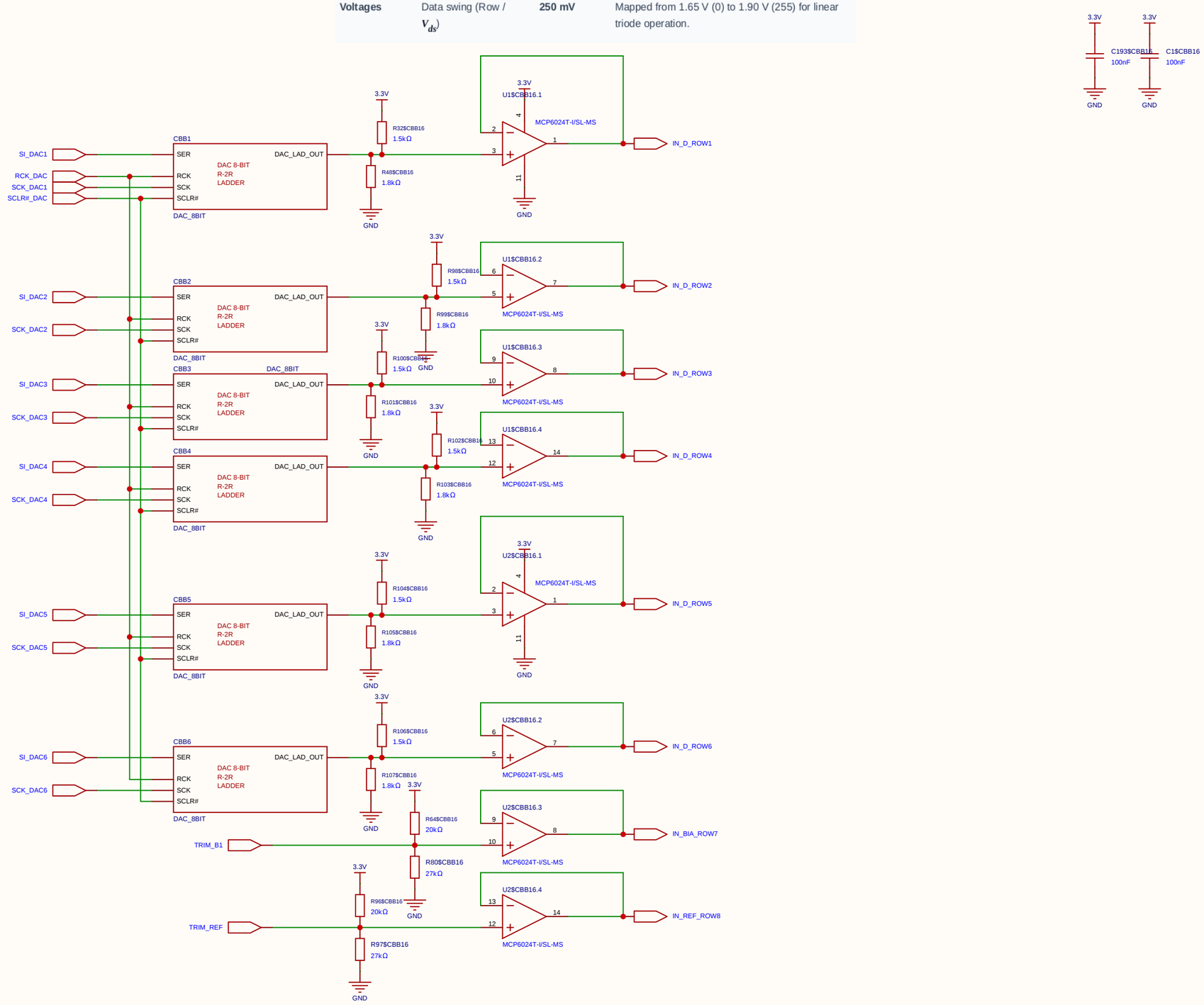
Schematic	SIGMOID_10	Create at	2026-06-19
		Update at	2026-06-19
Board		Page	SIGMOID(10)
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

$$V_{ut_TIA} = 1.65\ \text{V} - (5\ \text{mA} \times 100\ \Omega) = 1.65\ \text{V} - 0.5\ \text{V} = \mathbf{1.15}\ \text{V}$$



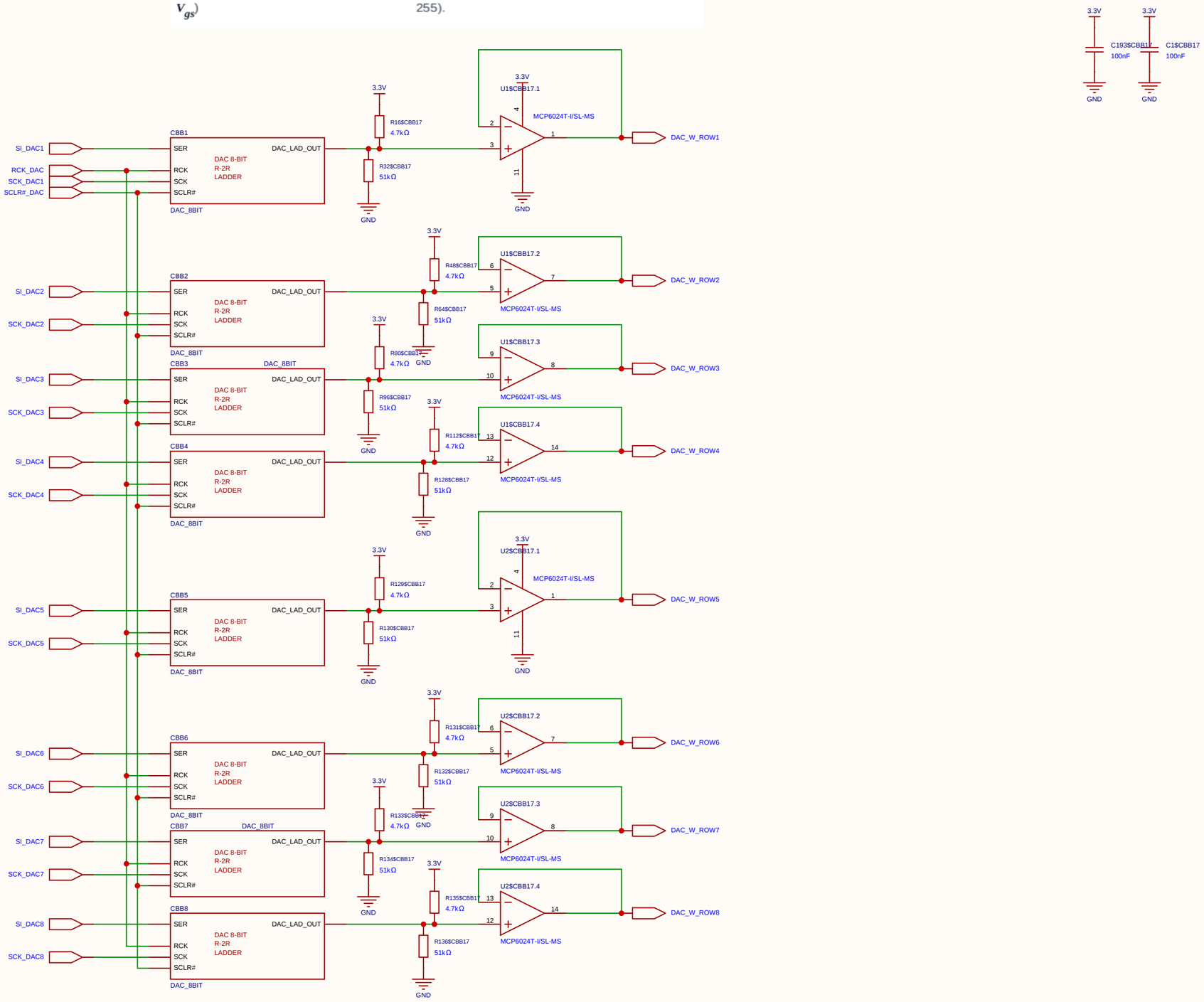
Schematic	matrix8	Create at	2026-06-25
		Update at	2026-06-27
Board		Page	matx8
Drawn		Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

Voltages	Data swing (Row / V_{ds})	**250 mV**	Mapped from 1.65 V (0) to 1.90 V (255) for linear triode operation.



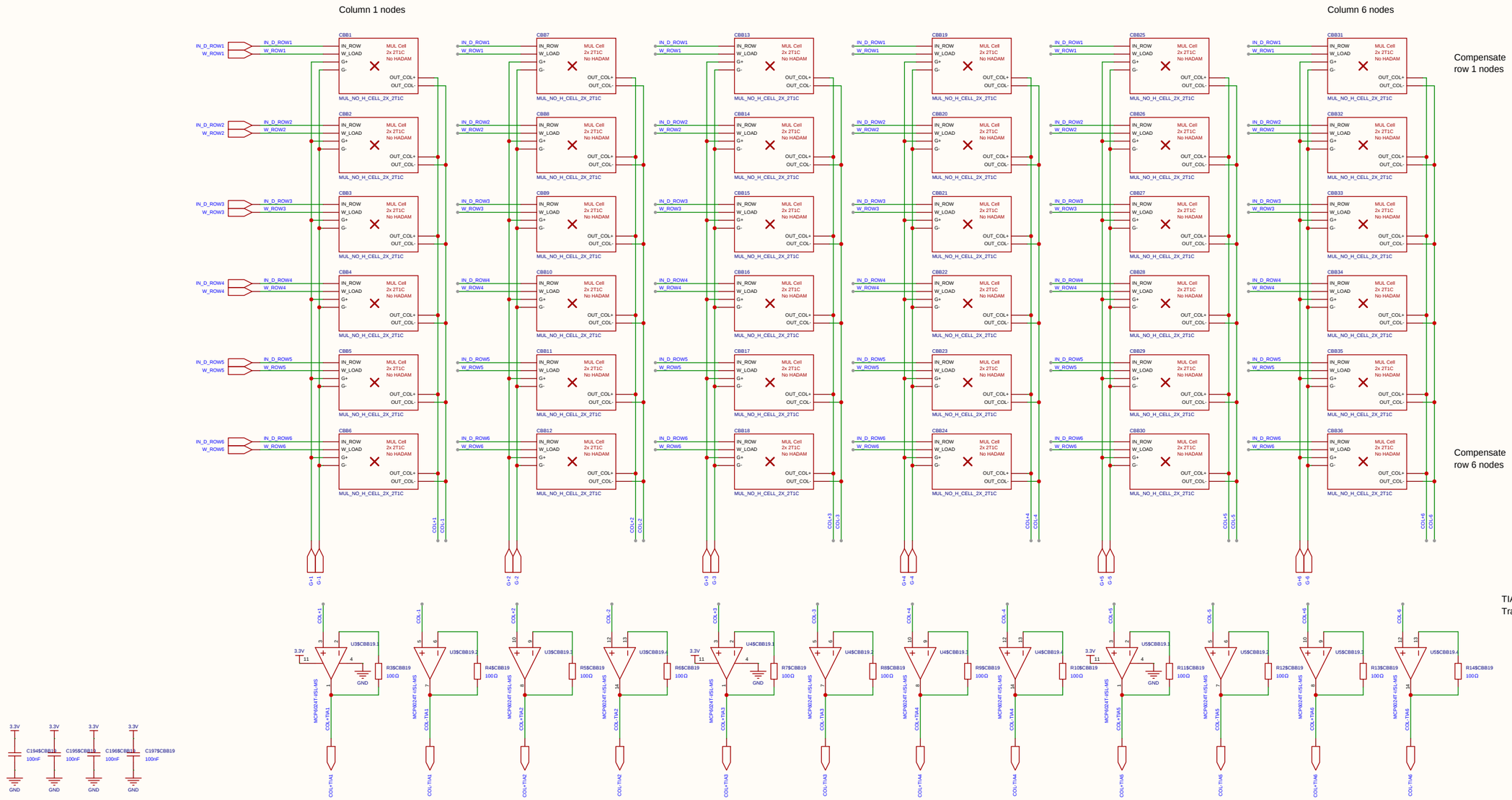
Schematic	6xDAC_DATA_ROWS	Create at	2026-06-20
		Update at	2026-06-20
Board		Page	6xDAC_8-bit
Drawn		Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

Weight swing (Gate / V_{gs})	**1.0 V**	Swings from 2.1 V (Weight 0) to 3.1 V (Weight 255).



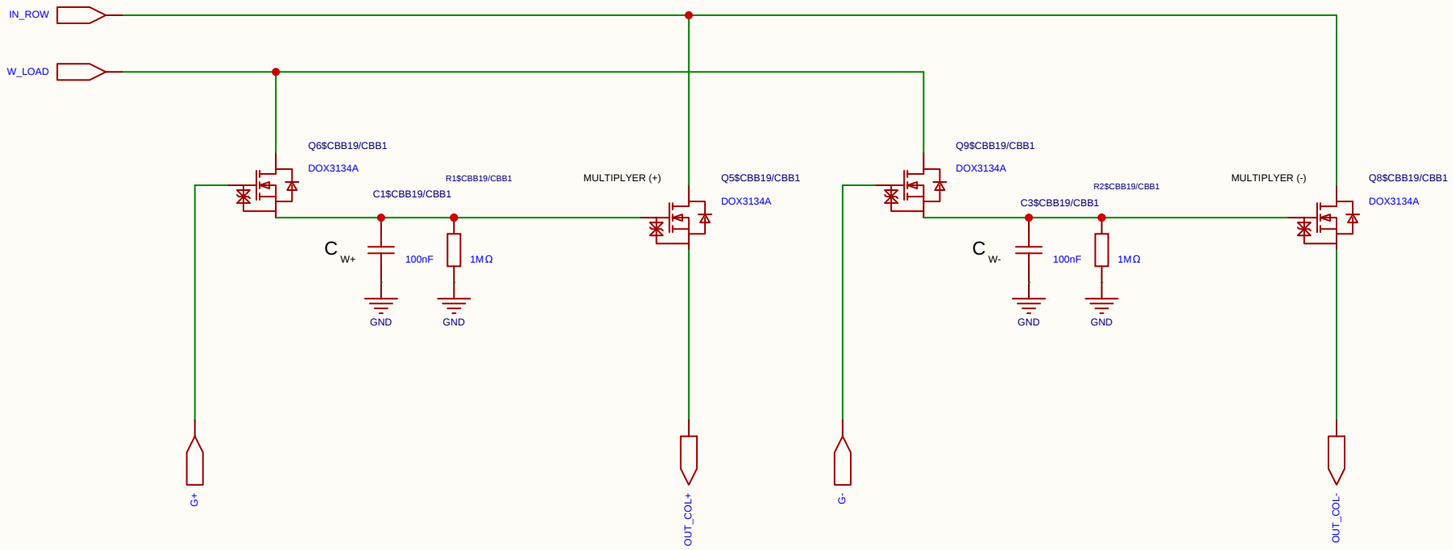
Schematic	8xDAC_WEIGHT	Create at	2026-06-19
		Update at	2026-06-30
Board		Page	8xDAC_8-bit
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

$$V_{ut_TIA} = 1.65\ \text{V} - (5\ \text{mA} \times 100\ \Omega) = 1.65\ \text{V} - 0.5\ \text{V} = \mathbf{1.15}\ \text{V}$$



Schematic	matrix33	Create at	2026-06-25
		Update at	2026-06-28
Board		Page	matx33
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

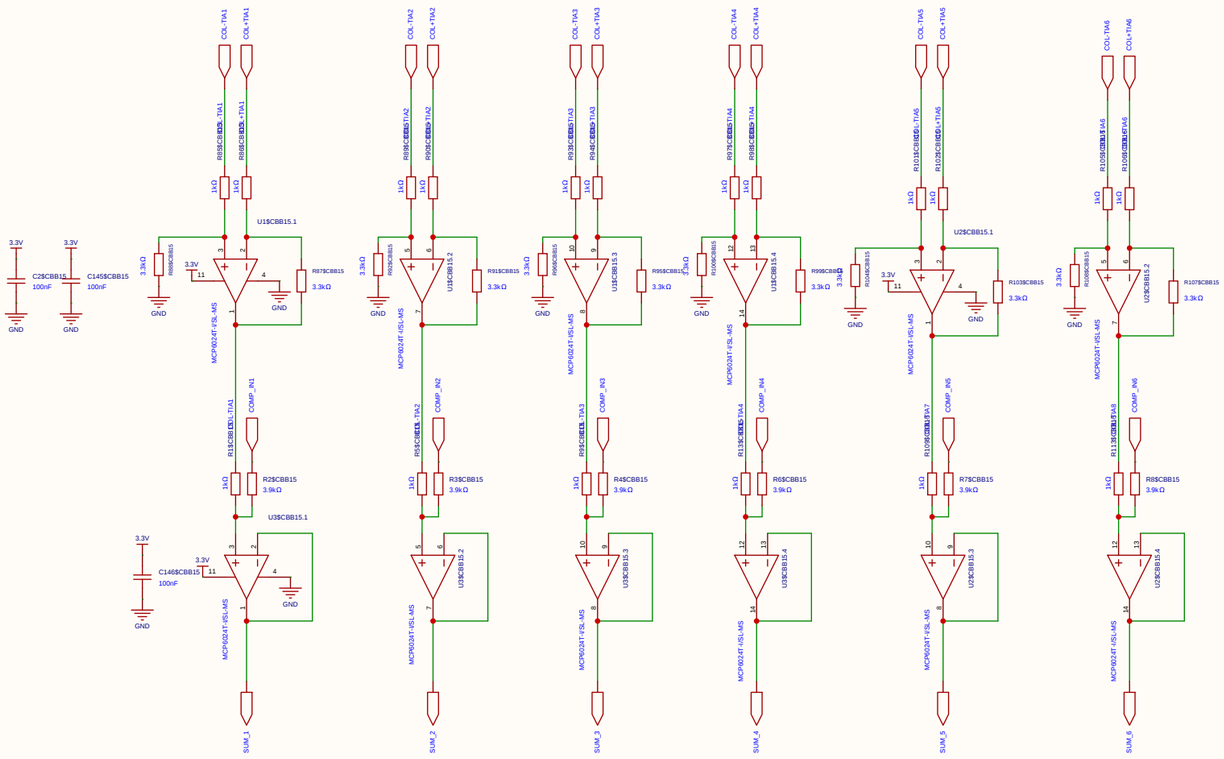
Analog Multiplication CELL Kernel
Differential 2x 2T1C



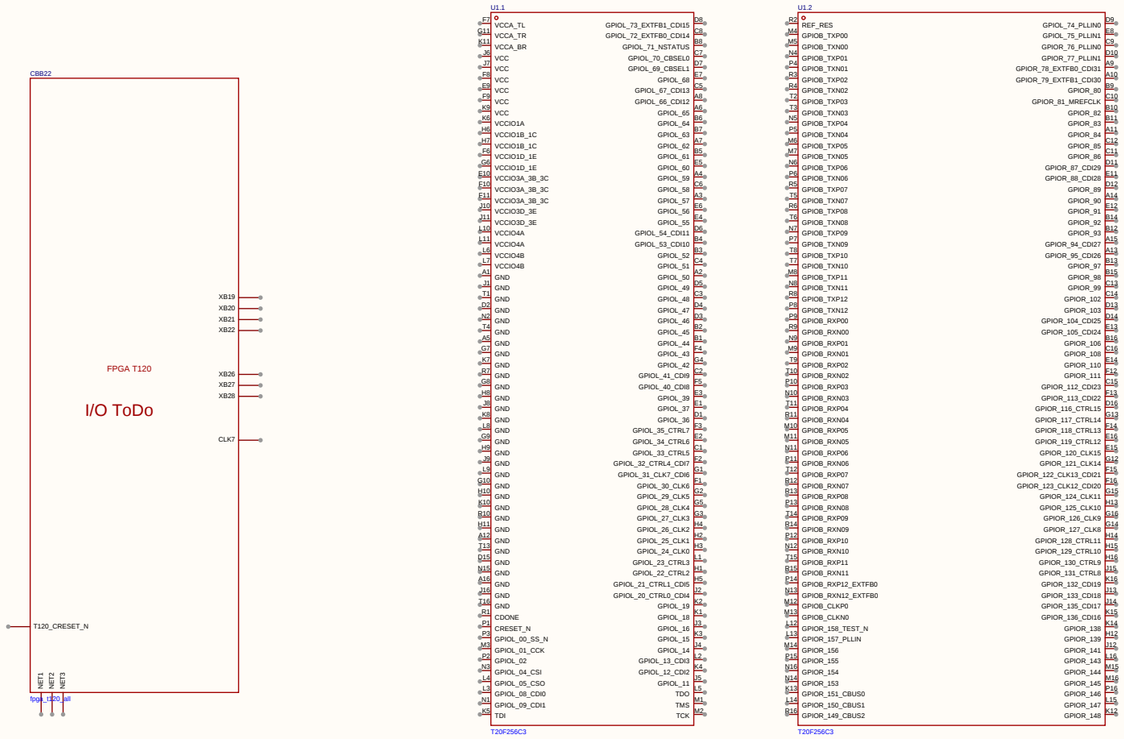
Schematic	MUL_NO_H_CELL_2X_2T1C	Create at	2026-06-20
		Update at	2026-06-28
Board		Page	matrix_33_MUL_CELL
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com

- **Calibration Example:** To match a 3.3 V ADC, the resistors are configured for a Gain of 6.6×.

  $V_{ADC} = 6.6 \times (1.65\ V - V_{out_TIA})$



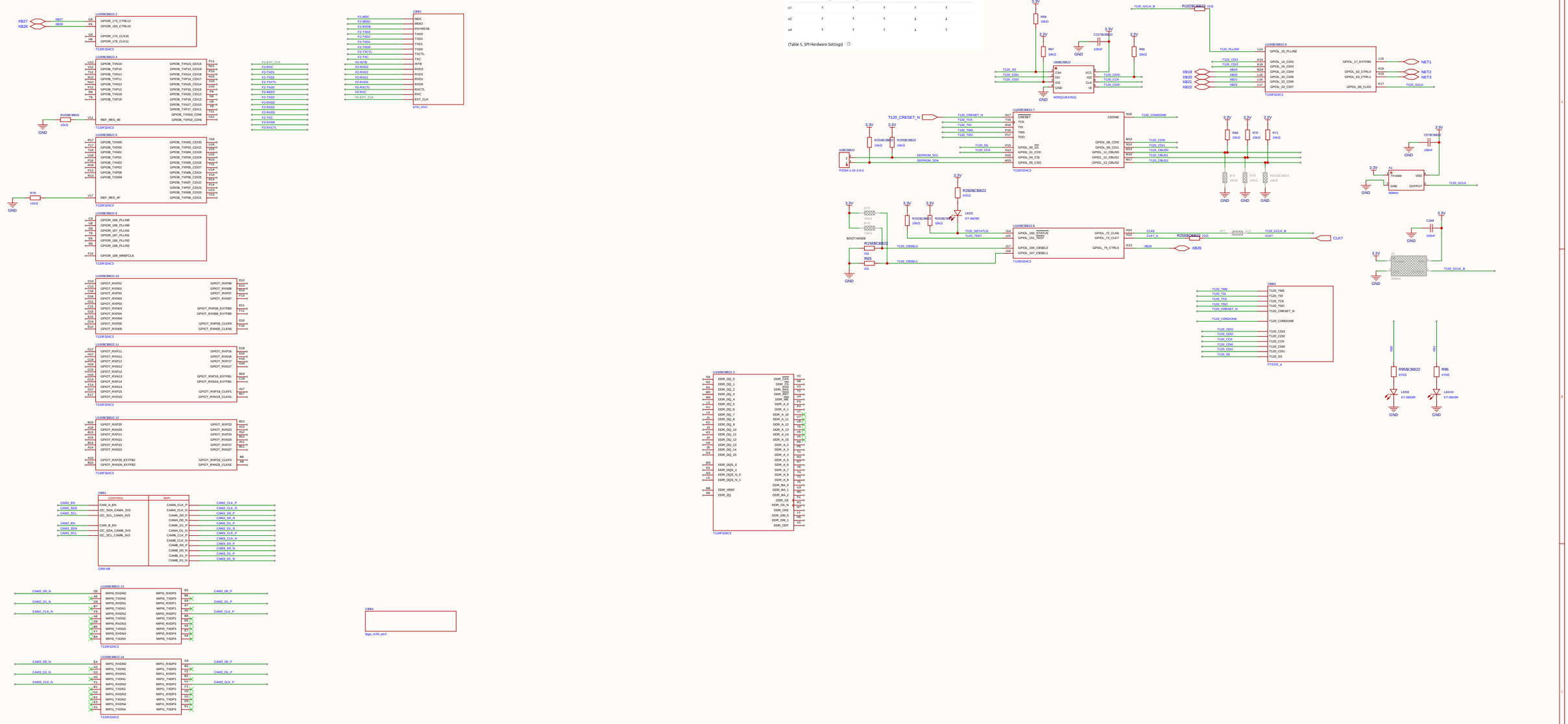
Schematic	SUM35	Create at	2026-06-19
		Update at	2026-06-19
Board		Page	sum35
Drawn	Olle Welin	Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com



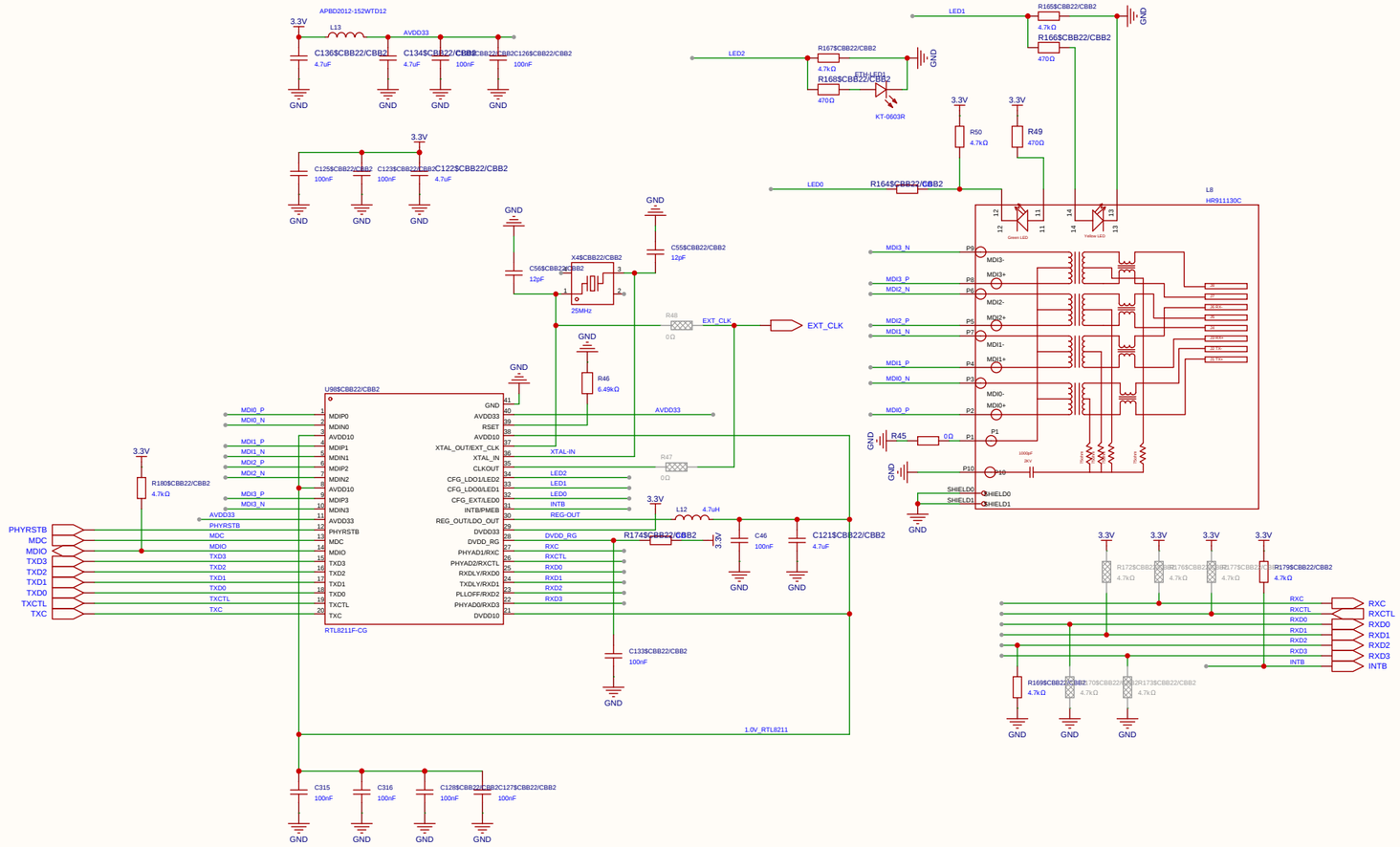
Schematic	Inverted_MAML	Create at	2026-06-25
		Update at	2026-06-25
Board	Analog_Matrix	Page	Digital_Controller
Drawn		Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 3 Total 3
EasyEDA		V1.0	A4	EasyEDA.com

Width	TEST_N	SS_N	CBUS2	CBUS1	CBUS0
x1	↑	↑	↑	↑	↑
x2	↑	↑	↑	↓	↓
x4	↑	↑	↑	↓	↑

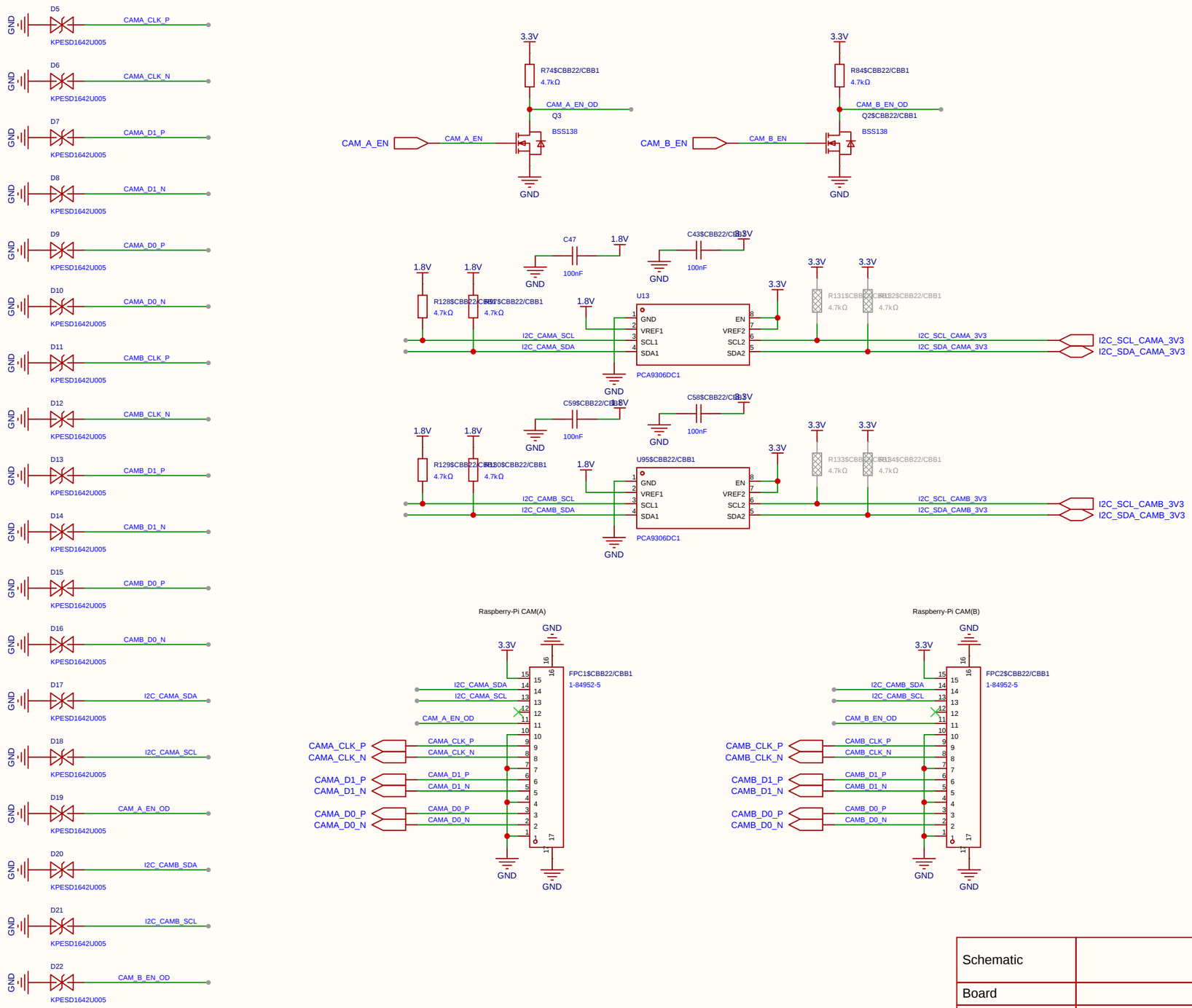
(Table 5, SPI Hardware Setting)



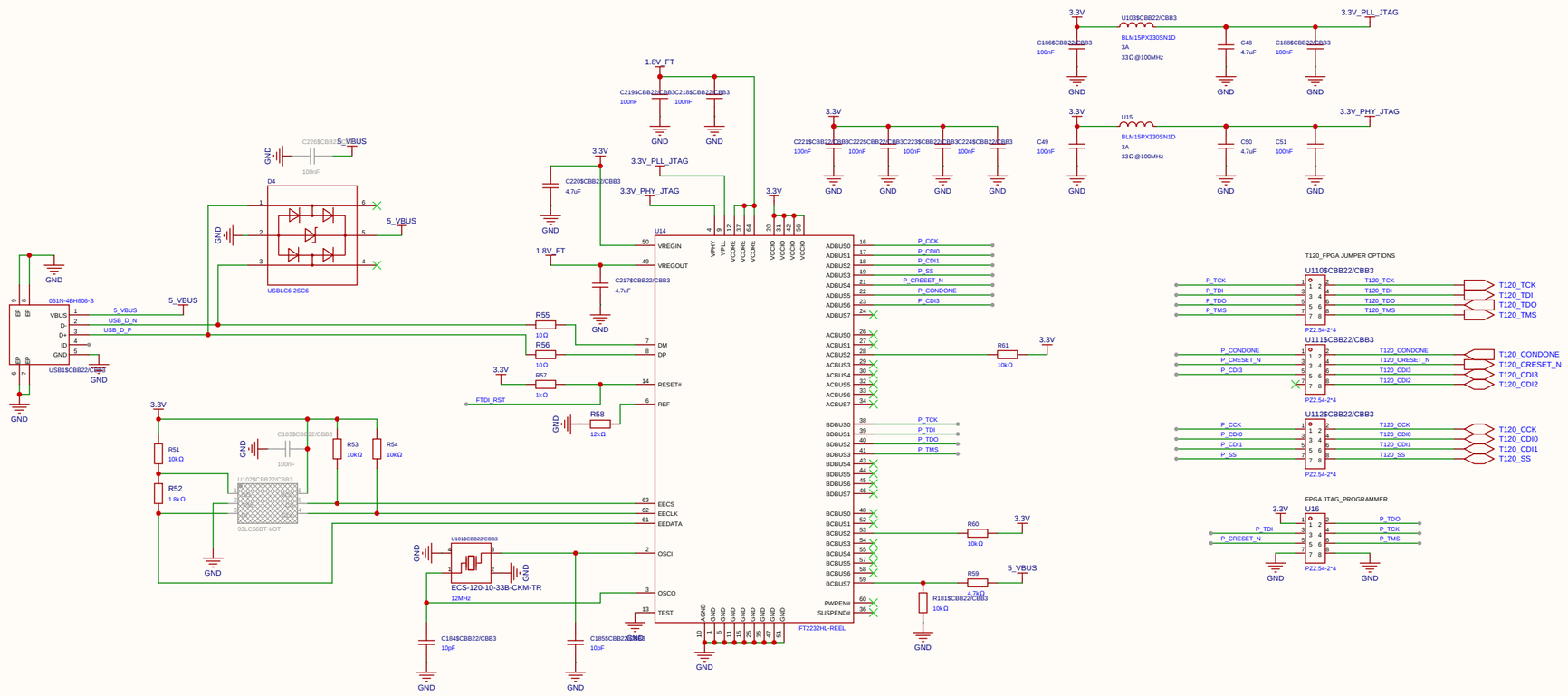
Schematic	fpga_t120_all	Create at	2026-06-25
Board		Update at	2026-06-30
		Page	P1
Drawn			
Reviewed		Inverted_MAML_6x6	
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com



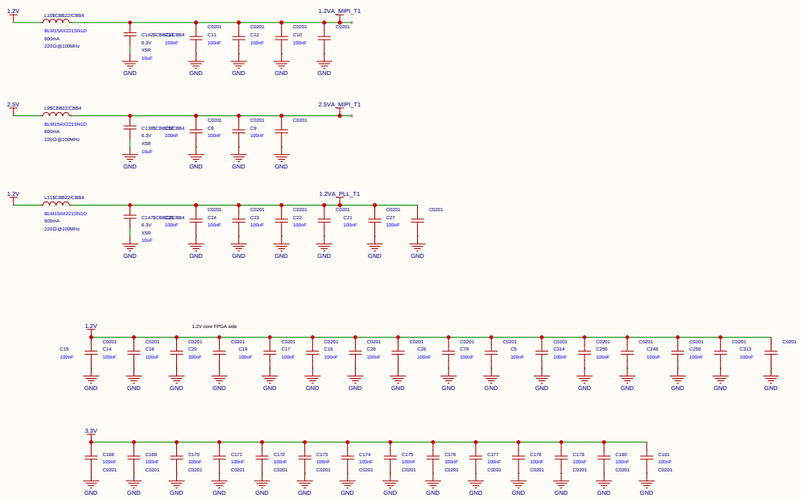
Schematic	ETH_PHY	Create at	2026-06-25
		Update at	2026-06-25
Board		Page	P1
Drawn	Inverted_MAML_6x6		
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com



Schematic	CAM-AB	Create at	2026-06-25
		Update at	2026-06-25
Board		Page	P1
Drawn		Inverted_MAML_6x6	
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com



Schematic	FT2232_a	Create at	2026-06-25
		Update at	2026-06-25
Board		Page	P1
Drawn	Inverted_MAML_6x6		
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com



Schematic	fpga_t120_etc2	Create at	2026-06-25
		Update at	2026-06-25
Board		Page	P1
Drawn	Inverted_MAML_6x6		
Reviewed			
		Version	Size	Page 1 Total 1
EasyEDA		V1.0	A4	EasyEDA.com